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Serial No.: 10/633,090   Attorney Docket No.: K35A1324

REMARKS

The Applicant thanks the Examiner for his careful and thoughtful examination of the present application. By way of summary, Claims 1-16 were pending in this application. Claims 1-3, 7-11 and 15 have been amended. Accordingly, Claims 1-16 remain pending for consideration.

CLAIM AMENDMENTS

Claims 2, 3, 7, 8, 10, 11 and 15 have been amended to clarify the claim language without altering their scope. These claim clarifications are not made for patentability purposes, and it is believed that the claims would satisfy the statutory requirements for patentability without the entry of such clarifications.

REJECTION OF CLAIMS 1-3, 7, 9-11 AND 15 UNDER 35 U.S.C. § 102(b)

The Office action rejected Claims 1-3, 7, 9-11 and 15 under 35 U.S.C. § 102 as being anticipated by U.S. patent no. 6,418,516, issued to Arimilli *et al.* (Arimilli). Applicant respectfully traverses this rejection because Arimilli fails to identically teach every element of the claims. *See* M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

Claim 1 has been amended to clarify one of the features distinguishing the claimed invention from Arimilli. Applicant submits that this claim would satisfy the statutory requirements for patentability without the entry of such clarification. However, as amended, Claim 1 now recites "providing the fetched non-instruction data to the micro-controller without caching the fetched non-instruction data." Arimilli neither teaches nor discloses this limitation.

The Examiner cites to two portions of Arimilli as allegedly anticipating this limitation of Claim 1. First, the Examiner cites to Fig. 6, steps 356 and 358 and Col. 11, lines 4-8 as teaching this limitation. The Examiner explains that the cache memory in

the claim is equivalent to the upper level cache, implying that Arimilli teaches providing fetched non-instruction data to the micro-controller while bypassing the upper level cache.

In fact, Arimilli does not teach or suggest such an embodiment. Instead, Arimilli teaches an improved method of caching speculative data. As taught at Col. 11, "[f]or speculative requests, if the request is not for an instruction fetch (356), if the lower cache is missed (358), only the lower level cache is loaded (362)." Col. 11, ll. 4-6. However, this method of loading only the lower level cache is only taught or suggested by Arimilli for speculative requests. Arimilli does not teach or suggest bypassing the upper level cache for non-instruction data provided to the micro-controller. Indeed, if the load request is not speculative but is instead a demand request for data that will be provided to the micro-controller (i.e., a request arising from an actual load or i-fetch operation), then both the upper-level and lower-level caches are filled as shown in Fig. 6, steps 352, 354, 364 and 366. Also see Col. 10, l. 67 – Col. 11, l. 4. Thus, Arimilli does not disclose or suggest providing the fetched non-instruction data to the micro-controller without caching the fetched non-instruction data.

The Examiner also makes a second argument that, as shown in Fig. 7 of Arimilli, if the requested data is non-instruction data that does not reside in the cache then the non-instruction data should bypass the instruction cache memory. The Examiner argues therefore that Claim 1 reads on the instruction cache in Arimilli.

Applicant respectfully submits that amended Claim 1 clarifies the claim language by more explicitly stating that the fetched non-instruction data is provided to the micro-controller without caching the fetched non-instruction data. In Fig. 7 of Arimilli, it is clearly illustrated that non-instruction data is cached in L1 Data Cache 306, and, as discussed above, Fig. 6 illustrates that non-instruction data is always cached before being provided to the micro-controller. Thus, Arimilli has a cache system that functions identically to the prior art systems discussed in Applicant's background: "[i]n prior art cache systems, a so-called "Harvard" architecture has been used which attempts to solve the foregoing problem by providing separate cache structures for instructions and

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data." Thus, Arimilli does not teach or suggest a method of providing fetched non-instruction data to the micro-controller without caching the fetched non-instruction data.

For at least these reasons, the rejection of Claim 1 as anticipated by Arimilli is improper.

Claim 9 has been amended similarly to Claim 1, and now recites a micro-controller cache system adapted to "provide the fetched non-instruction data to the micro-controller without caching the fetched non-instruction data." Arimilli neither teaches nor discloses such a system.

For reasons similar to those discussed above with respect to Claim 1, Applicant submits that Arimilli does not teach or suggest a micro-controller cache system adapted to provide the fetched non-instruction data to the micro-controller without caching the fetched non-instruction data. For at least these reasons, the rejection of Claim 9 as anticipated by Arimilli is improper.

Claims 2-3 and 7, and Claims 10-11 and 15, which depend from Claims 1 and 9 respectively, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 9, and because of the additional features recited therein.

REJECTION OF CLAIMS 4-6, 8, 12-14 AND 15 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 4-6, 8, 12-14 and 16 under 35 U.S.C. § 103 as being unpatentable over Arimilli in view of U.S. patent application publication no. 2002/0065994, by Henson et al. (Henson).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

The Applicant respectfully traverses this rejection because Arimilli alone or in combination with Henson, fails to teach or suggest all of the elements of independent Claims 1 and 9, as discussed above. See M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must

teach or suggest <u>all</u> the claim limitations). Henson does not teach any of the limitations discussed above that were not taught or suggested by Arimilli.

Claims 4-6, 8, 12-14 and 16, which depend from Claims 1 and 9, are therefore believed to be patentable for the same reasons articulated above with respect to Claims 1 and 9, and because of the additional features recited therein.

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CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: July 10, 2006

By: _____
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